

# ASTEP

Altitude SEE Test European Platform  
Resp. L2MP:JL Autran

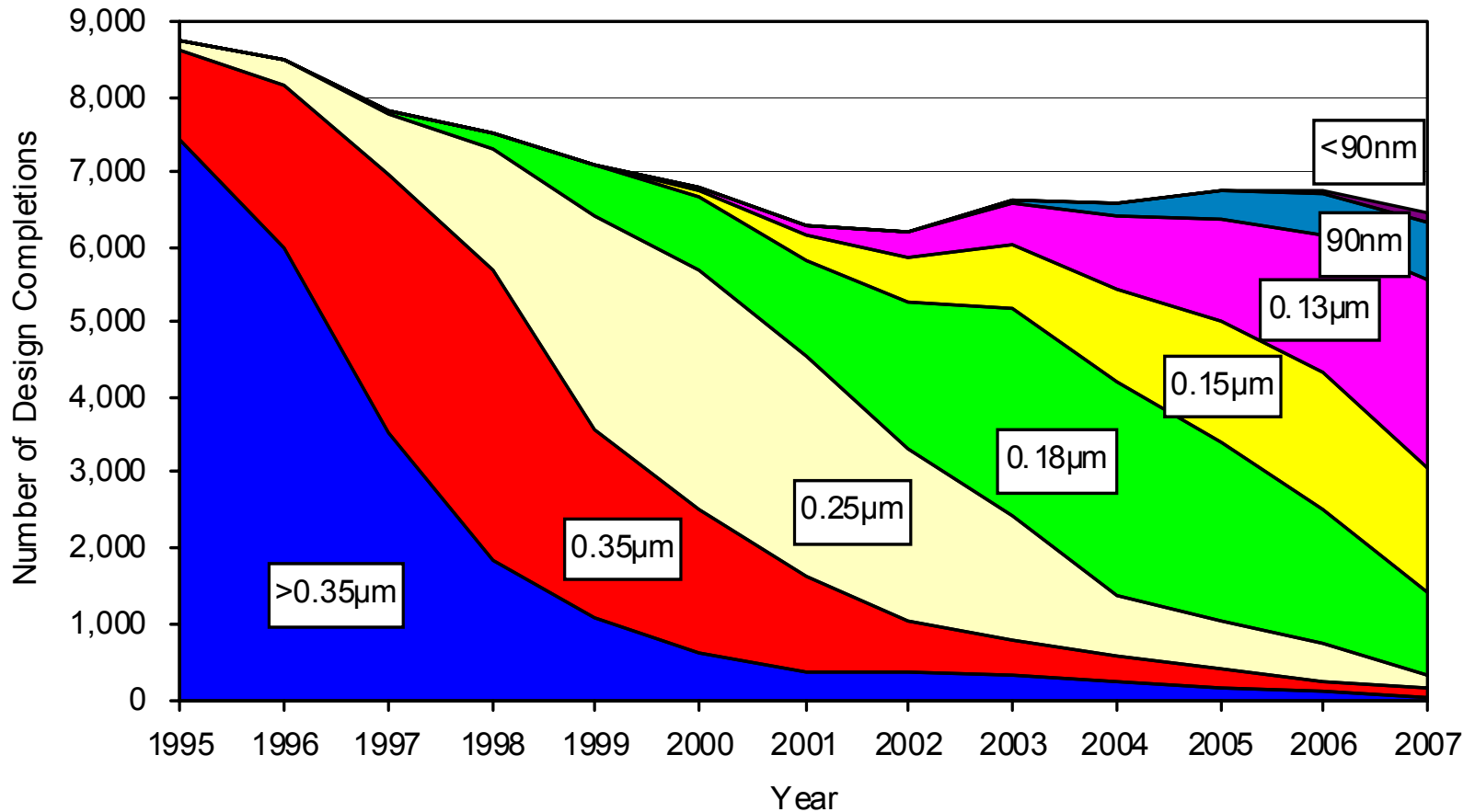
J. Borel

JB-R&D

# Problem statement

- The move of ICs technologies to nanometer dimensions leads to a significant decrease of electric charges on the logic nodes (#fcb).
- Cosmic Rays of the natural environment hitting the device create much higher amount of charges impacting its logic behavior.

# DESIGN COMPLETIONS BY FEATURE DIMENSION

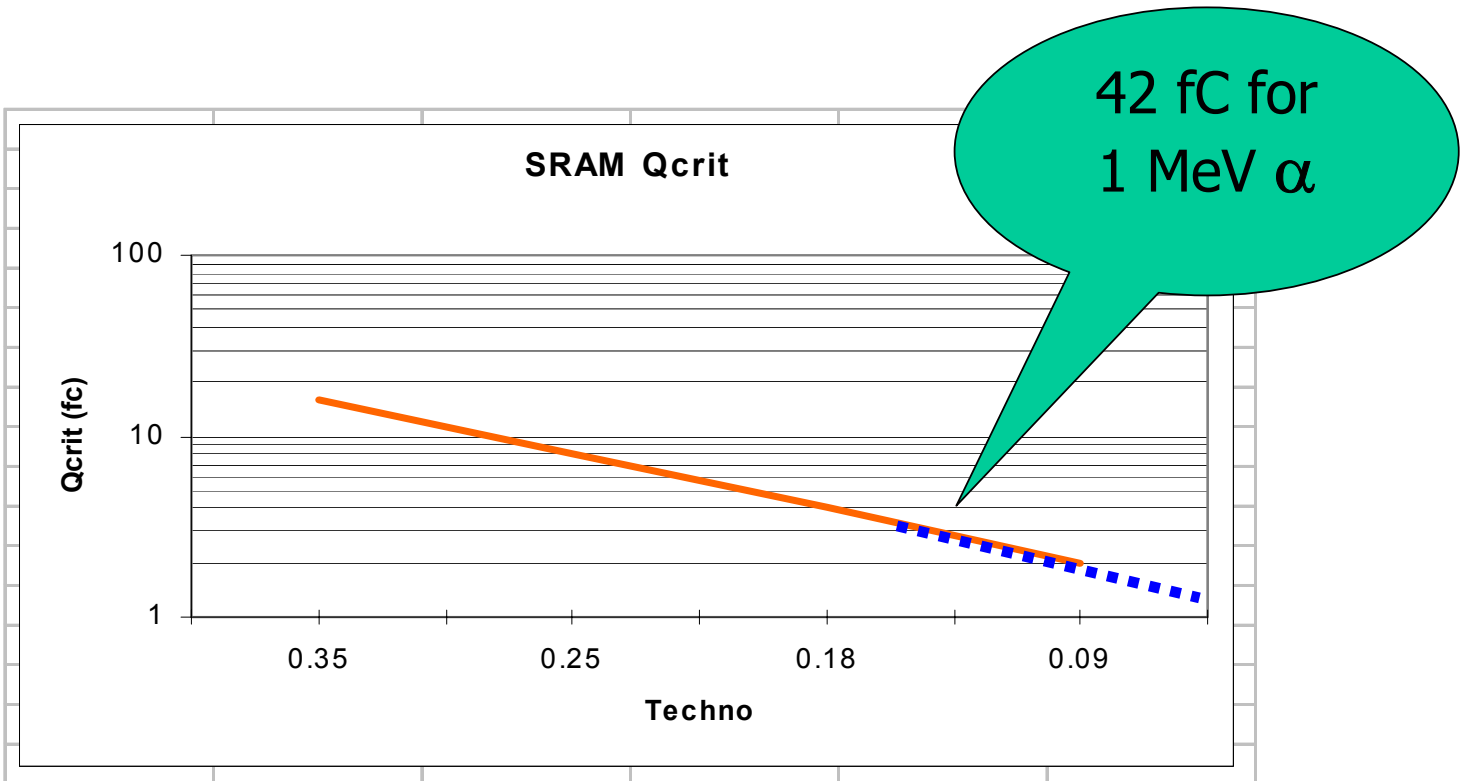


**SLOWING OF MIGRATION TO NEW TECHNOLOGIES**



MS-MEDA11.043

# Critical Charge Evolution



# Consequences

- Low power circuits (communicating objects, pacemakers, personal assistants ...) are more sensitive.
- A wrong behavior of the device can lead to a drastic situation in medical, banking transactions, telecom routers...

# Technical Aspects

# Alpha and neutron accelerated tests on 130nm-ST chips

- Carried out on STMicroelectronics test chips, the same used for ASTEP
- Accelerated test done at the TRIUMF cyclotron accelerator, Vancouver
- Continuous neutron flow, alpha source Am241.

## Test Set-up

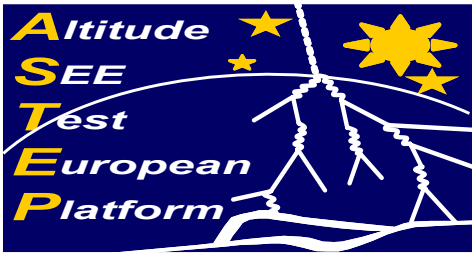
- Different bias supplies per DUT
- programmable Ios
- SEL protected

## Device test conditions

- 3 different patterns : Checkerboard, All1, All0
- Static/dynamic test
- VDD from 0.9 to 1.5V
- Room temperature and specific tests at 125°C
- DUT tilt angle backside and frontside.



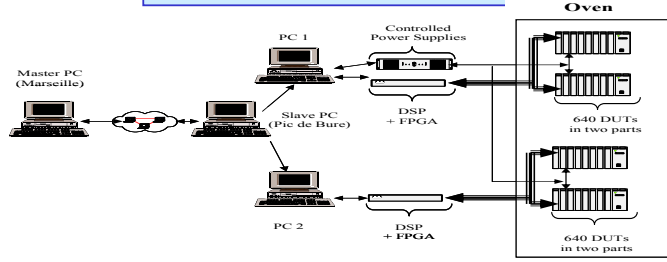




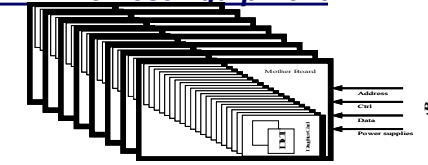
# ASTEP EXPERIMENTAL PROGRAM

## REAL-TIME SER MEASUREMENTS

The real-time SER measurement system developed in collaboration with Bertin Technologies (Aix-en-Provence) is a dedicated system capable of monitoring hundreds of chips over a large period of time. The system perform operations such as writing/reading the chips, comparing the output data to the written data, and recording details on induced errors.

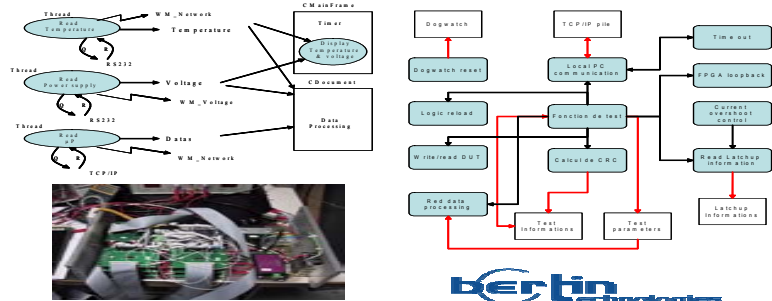


### ASTEP Life Test Equipment



2 DUTs per daughter card  
 20 daughter cards per mother board  
 8 mother boards on each rack  
 4 racks, 1280 DUTs in total

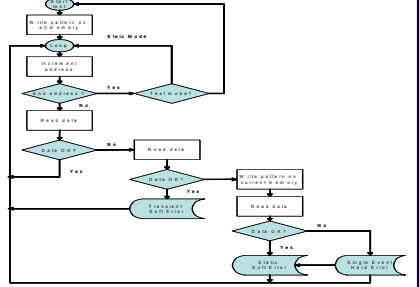
### PC and Processor Architectures



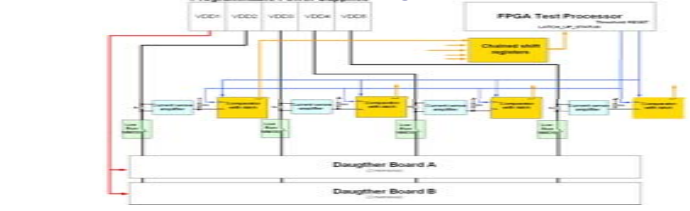
### Procedure of SEU Recognition

The procedure strictly follows the specifications and requirements of the JEDEC standard.

- Data writing (32 bits) with selected pattern
- For each memory point, Writing and rereading with data control
- If data correct, go test the next memory point
- If data state not correct, try to reread twice the data
- If data correct after rereading, error identified as "Transient Soft Error"
- If data still not correct, test twice to rewrite and to reread.
- If control valid after rewriting and rereading, error identified as "Static Soft Error"
- If control not valid after rewriting and rereading, error identified as "Single Event Hard Error"



### SEL Detection and Monitoring

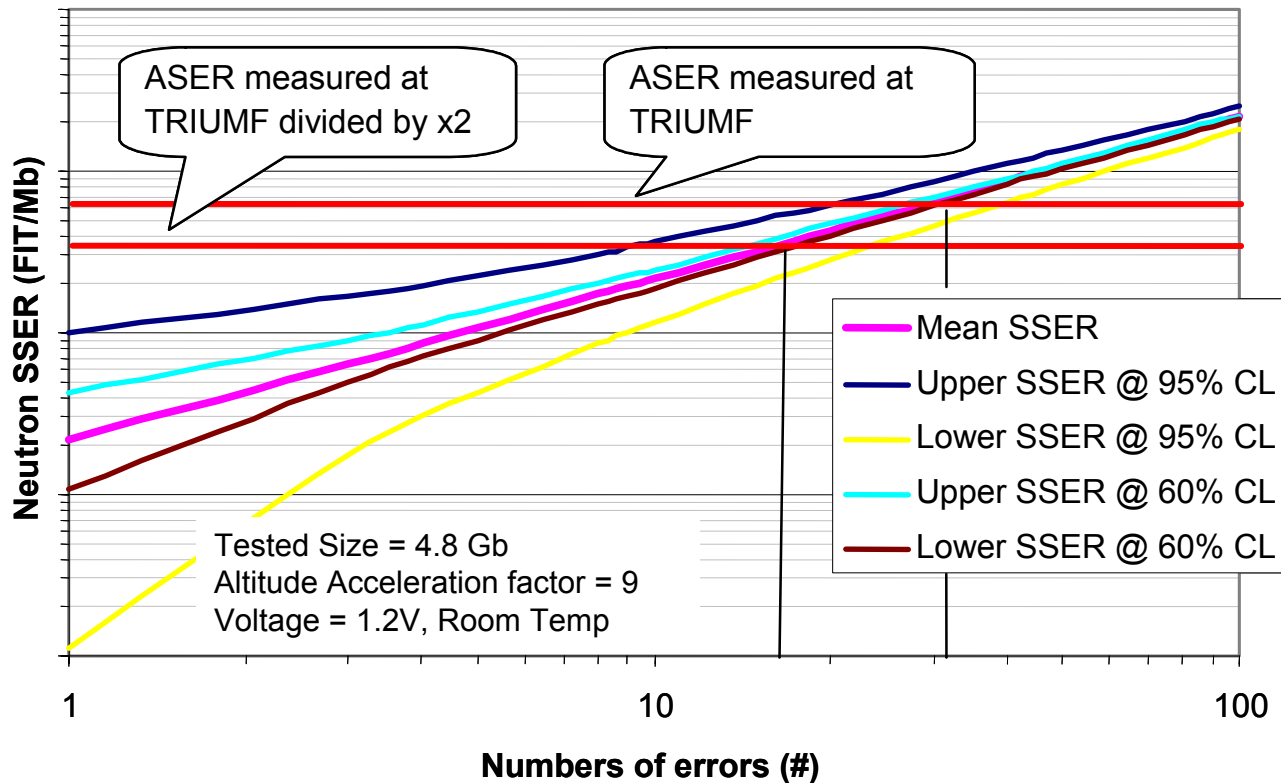


### Software interfaces



# From Accelerated to Real-Time

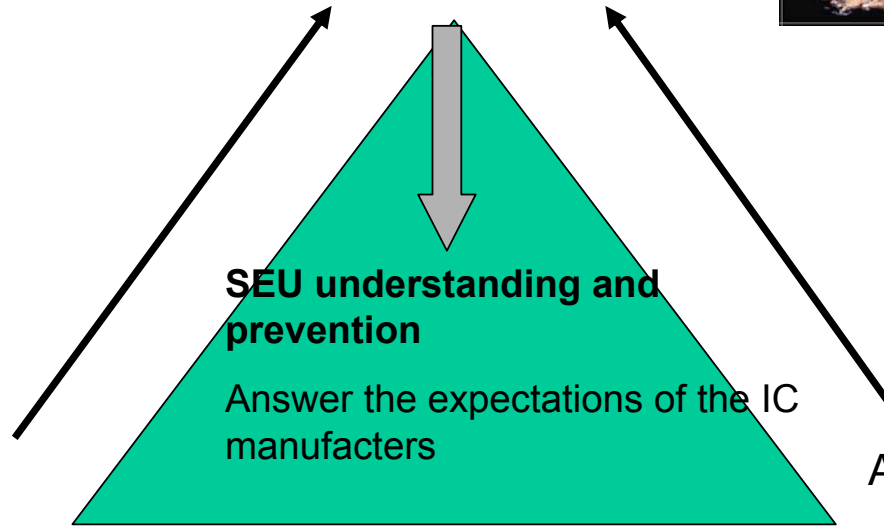
## SSER as a function of the number of errors for 90 days of test



15 to 30 errors expected at 2550m in the case of 130nm-ST devices previously tested at TRIUMF. Real-time tested results expected for spring 2006.

# ASTEP Vision

Cross simulation tools development



**SEU understanding and prevention**

Answer the expectations of the IC manufacturers

Alpha and neutron accelerated test

*Develop Real Time Testing to calibrate accelerated test results*



# The Pic de Bure project

# ASTEP building on Pic de Bure

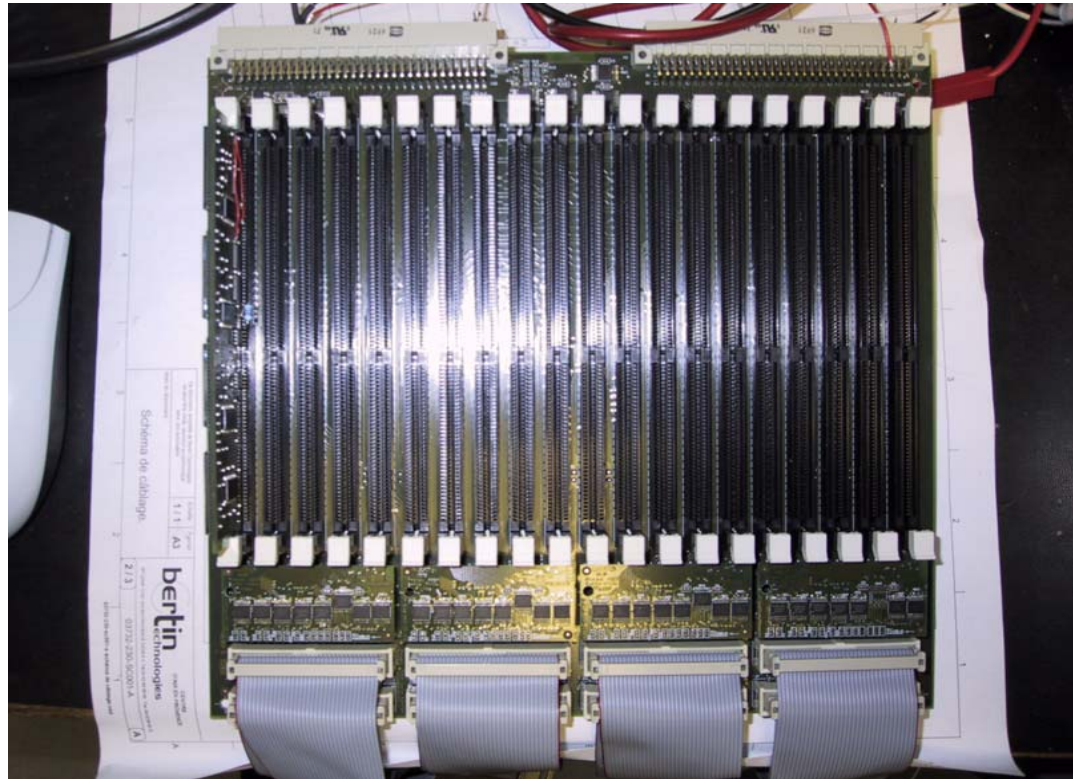


OCOVA 2005                      Forum  
Objets Communicants & valorisation

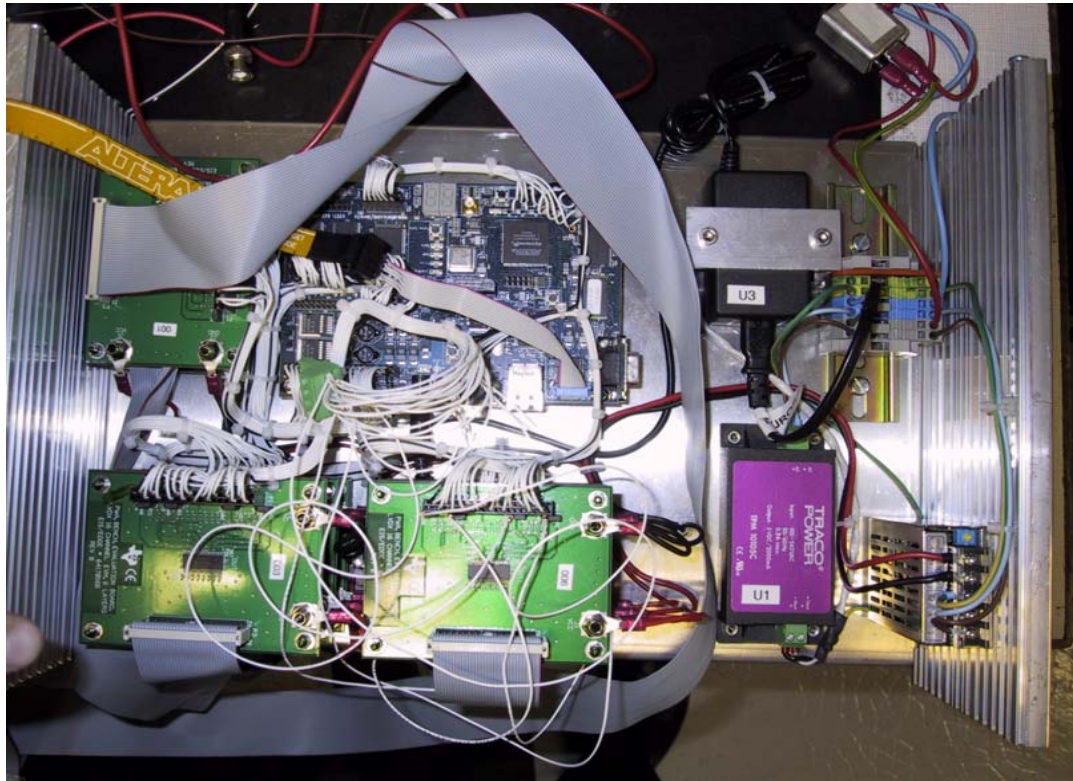
# Tester room on Pic de Bure (VPN remote picture)



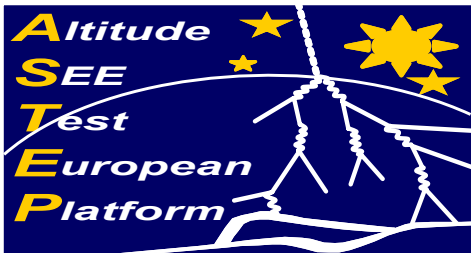
# Mother Board for 20 daughter cards, i.e. 40 DUTs



# Control system



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Objets Communicants & valorisation



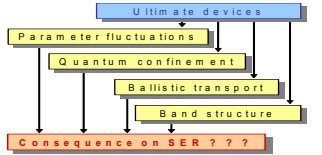
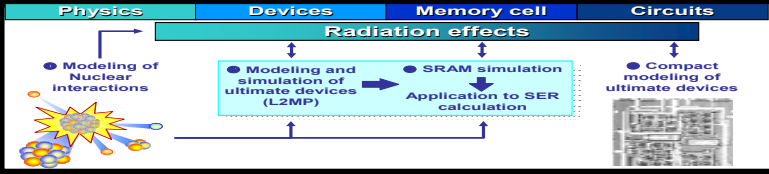
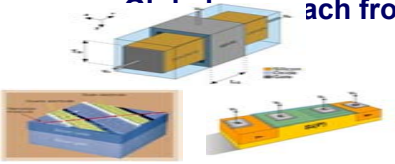
# ASTEP SIMULATION PROGRAM

## FROM NUCLEAR AND SEMICONDUCTOR PHYSICS TO DEVICES AND CIRCUITS

In complement to the experimental SEE characterization program and the development of the "Pic de Bure" facilities, ASTEP Simulation Program is a CNRS/L2MP initiative to develop predictive SER simulation codes, in collaboration with other academic laboratories and industrial partners.

### Main Objectives and Approach

- Correlate experiments and simulation on state-of-the-art technologies
- Predict SER for "end-of-the-roadmap" devices and circuits
- Investigate by simulation SER in alternative post-roadmap technologies



### CNRS/L2MP Numerical Simulation Platform

L2MP laboratory offers unique computational resources, at the French academic level, to perform heavy 2D or 3D numerical simulations of devices, circuits and systems on state-of-the-art workstations and clustered multi-processors PCs

**Investigate SEE in next ITRS Technology Nodes**

3D Simulation of GAA MOSFET under transient irradiation

Electron density (Quantum level)

SEU simulation in Double-Gate SRAM Cell (ICMTD'05)

**11 workstations SUN Blade (100, 1000, 2000)**  
**1 workstation HP J6000 bi-processors**  
**1 Cluster SUN 20 nodes 4Go/bi-opteron 2.2GHz**  
**1 Cluster SUN 6 nodes 32Go/bi-opteron 2.2 GHz**  
**+ 40 networked Windows PC (control workstations)**

**Simulation tools and platforms:**  
 SILVACO, ISE, Cadence, Mentor Graphics, Mathematica, Matlab, Femlab, Fortran 90, C, C++  
 Parallel libraries, meta-languages and control softwares

**Explore "end-of-the-roadmap" CMOS devices using atomistic models and simulations**

Gate-All-Around Si Nanowire MOSFET (ESSDERC'05)

**TIGHT-BINDING**

**NEGF Formalism**



# Status of R&D implementation

- Testing room operational (secured power supply, internet connection...).
- Silicon components available (from ST) and tested (10 giga+ of memory).
- Tester qualification nearly completed.
- Neutron detector selection in progress.
- Operational testing start: December 2005.

# General program: R&D and industrialisation at Sept. 2005.

- R&D program:
  - preparation phase completed.
  - Tests to start in December 2005.
- Industrial program definition:
  - based on evaluation results in the R&D program.
  - to start during Q1 2005.

# Supporting organisations

- CNRS/L2MP responsible for R&D programs.
- Supports received from:
  - Europe.
  - PACA region.
  - CG05 general council.
  - Mairie de St Etienne en Dy.